Using RTL-to-C++ translation for large soc co engineering: a case study

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A Ghosh, J Kunkel, S Liao - Proceedings of the conference on Design, automation and test ..., 1999 - portal.acm.org
... translation time, but eliminates bugs during **translation** which can ... sub- typing and
virtual function facilities of **C++**. ... similar to always blocks in **Verilog** or a ...
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... circuits and systems using C/**C++**, perform functional sim- ulation, and then **translate**
the portion ... description language (HDL), such as **Verilog** HDL or ...
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A C++ ASIC Design Methodology Facilitated by a **C++-Verilog** Translator
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... We decided to investigate tools for **C++** to **Verilog translation**. In ... The L1
C++ code was then ready for **translation** to **Verilog**. For ...
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... convert the C or **C++** description to **Verilog** or VHDL ... Or they do not support the
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... co-simulation of C and **Verilog** HDL or ... In a C/**C++**-based methodology, designer
productivity can ... significantly because one can eliminate **translation** from a ...
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... is dominated by the use of **Verilog** and VHDL ... **C++** extends the basic computational
facilities in C to ... Technically, **translating** C directly into silicon is not a ...
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System and method for system level and circuit level modeling and design simulation using C++ - group of 3 »
S Hsiao, S Tjiang, R Gupta - US Patent 6,152,612, 2000 - Google Patents
... 235 C++ Library: Timing Constructs Thread / Co-Routine Library 127) 220 ... 720 FIG.
1 1A /* **translation** to char */ const char stdjjlogic: :to_char_table [Ns1] = ...
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